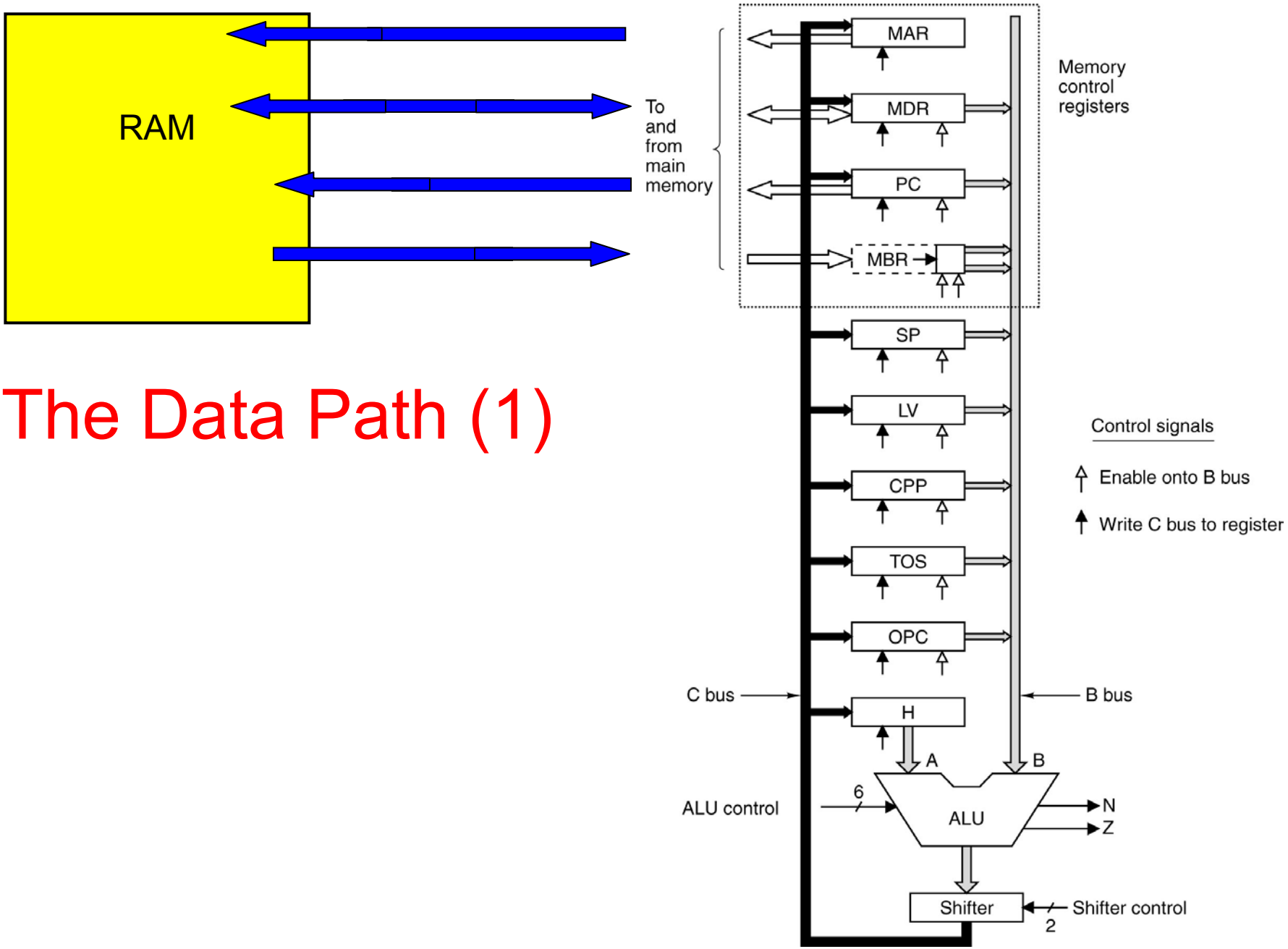
The Microarchitecture Level

Chapter 4

The Data Path (1)

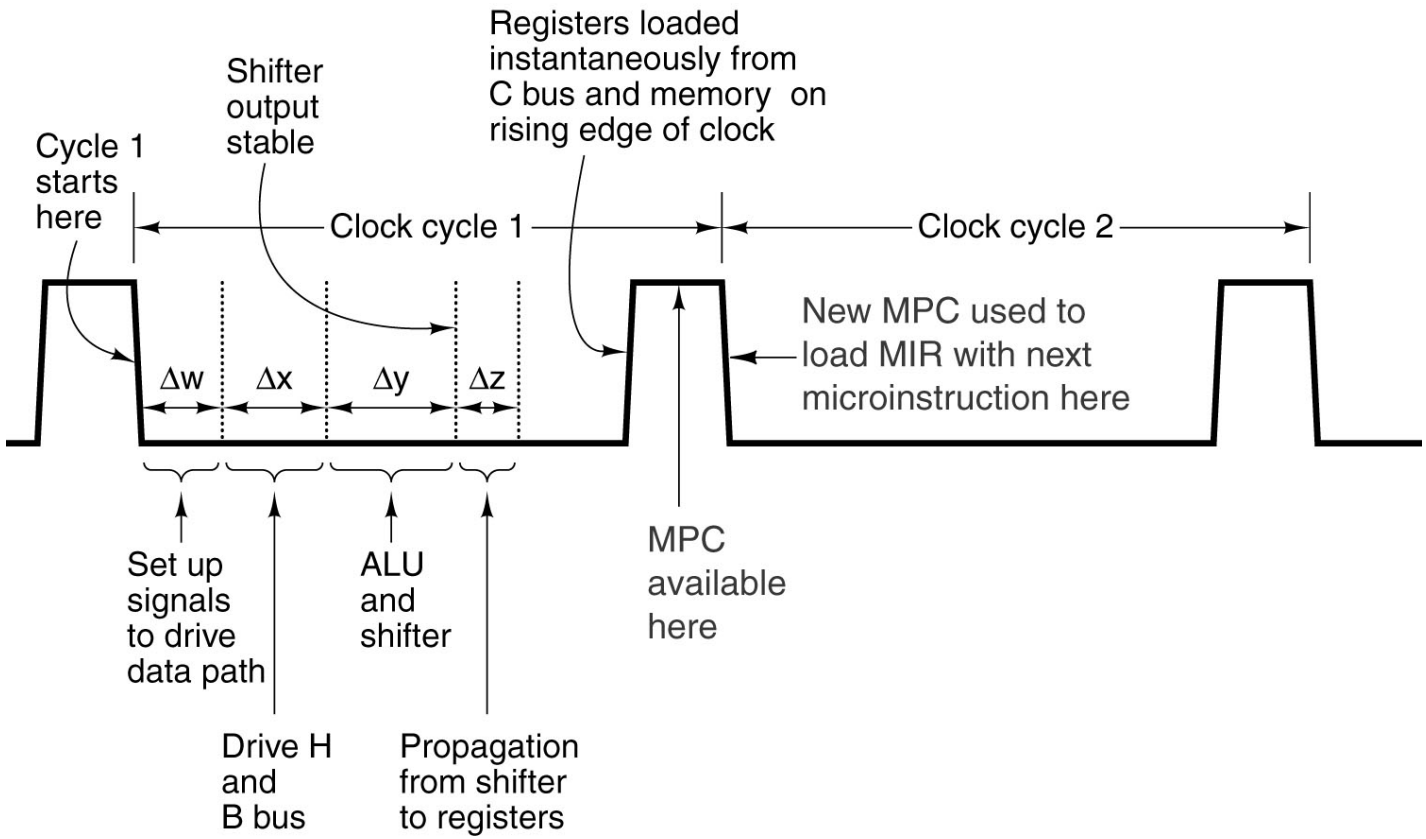


The Data Path (2)

F_0	F_1	ENA	ENB	INVA	INC	Function
0	1	1	0	0	0	A
0	1	0	1	0	0	B
0	1	1	0	1	0	$\overline{A}$
1	0	1	1	0	0	$\overline{B}$
1	1	1	1	0	0	A + B
1	1	1	1	0	1	A + B + 1
1	1	1	0	0	1	A + 1
1	1	0	1	0	1	B + 1
1	1	1	1	1	1	B – A
1	1	0	1	1	0	B – 1
1	1	1	0	1	1	–A
0	0	1	1	0	0	A AND B
0	1	1	1	0	0	A OR B
0	1	0	0	0	0	0
1	1	0	0	0	1	1
1	1	0	0	1	0	–1

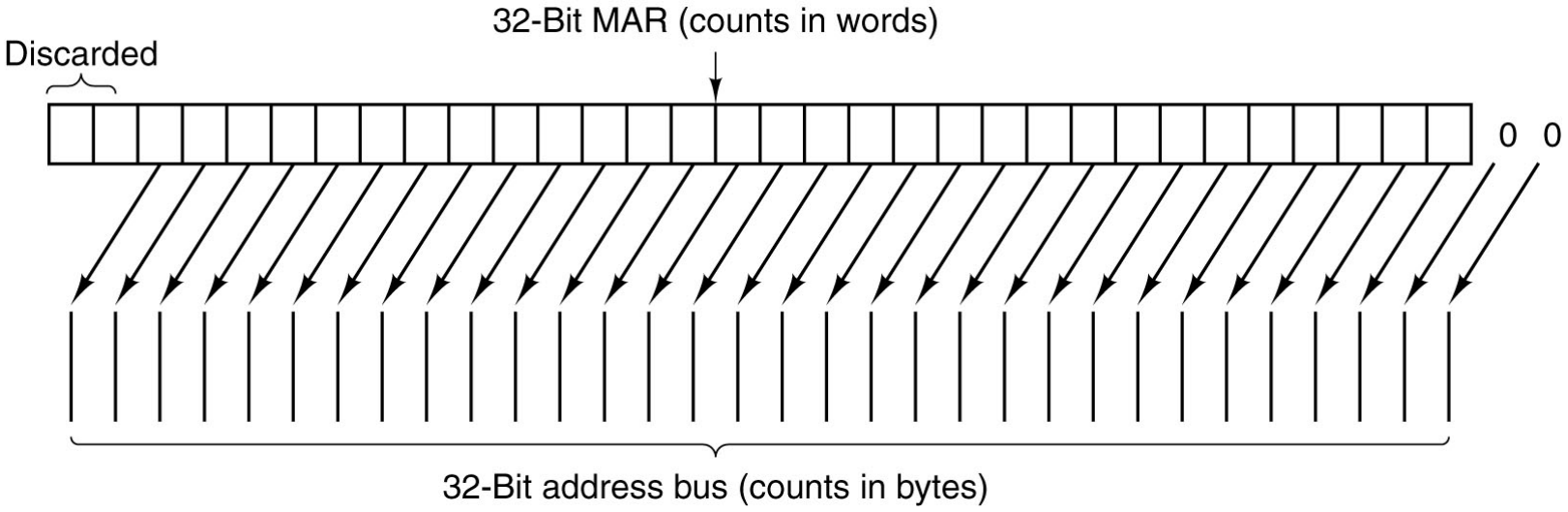
Useful combinations of ALU signals and the function performed.

Data Path Timing



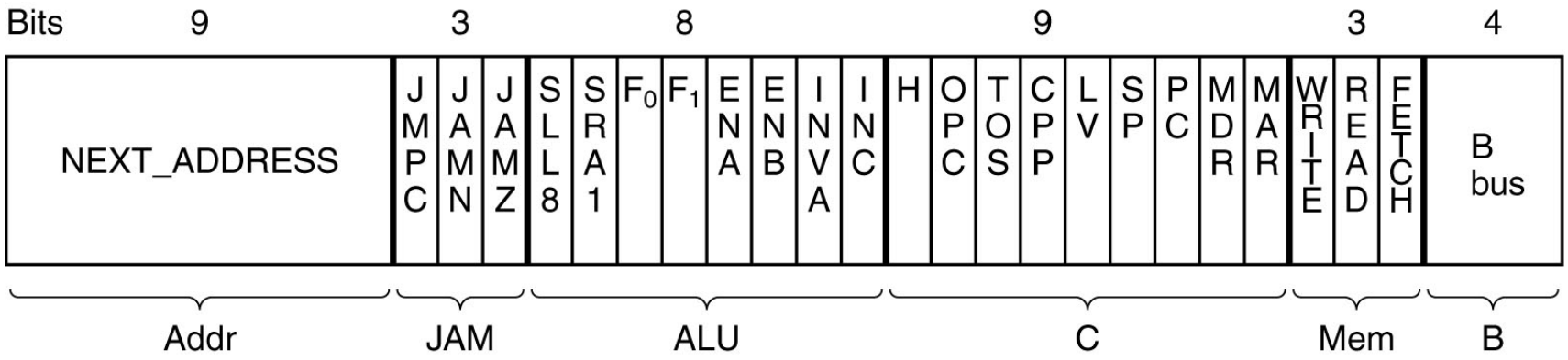
Timing diagram of one data path cycle.

Memory Operation



Mapping of the bits in MAR to the address bus.

Microinstructions



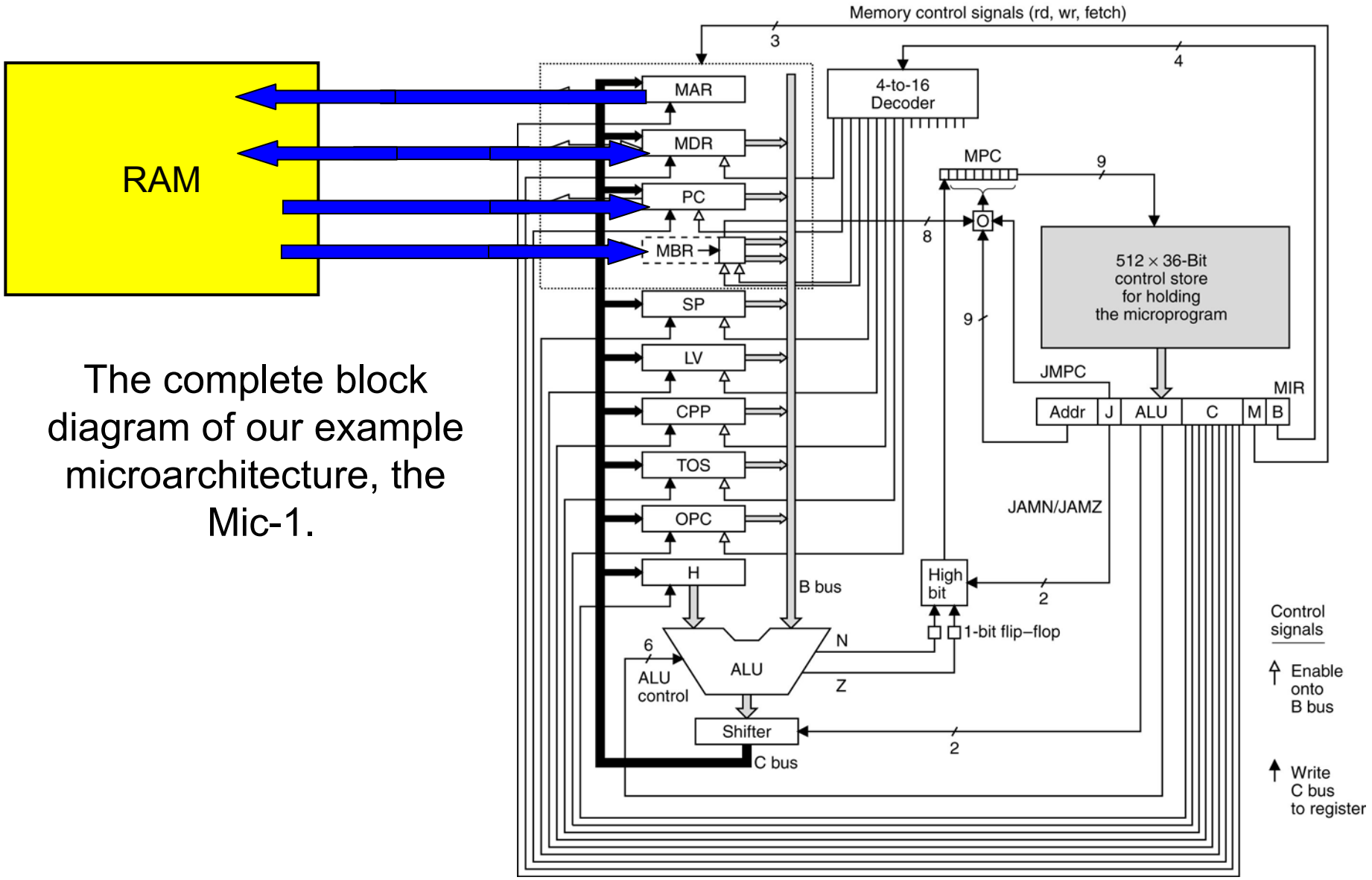
B bus registers

0 = MDR	5 = LV
1 = PC	6 = CPP
2 = MBR	7 = TOS
3 = MBRU	8 = OPC
4 = SP	9-15 none

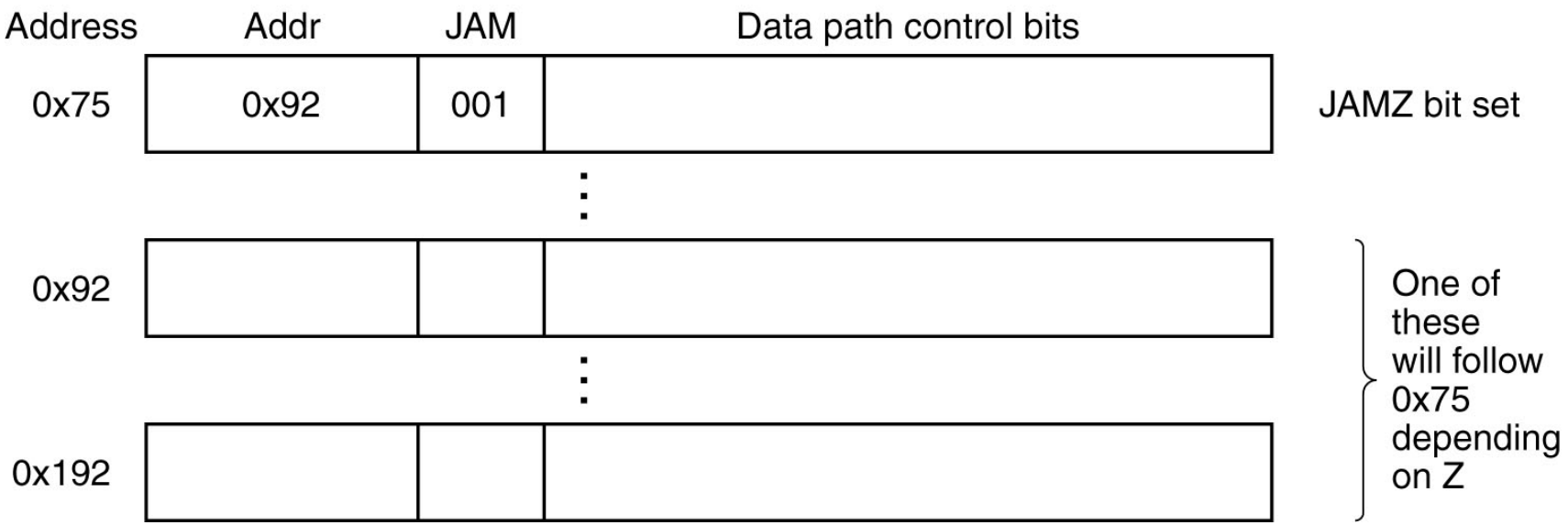
The microinstruction format for the Mic-1.

Microinstruction Control: The Mic-1 (1)

The complete block diagram of our example microarchitecture, the Mic-1.



Microinstruction Control: The Mic-1 (2)



A microinstruction with JAMZ set to 1 has two potential successors.