

Instruction Set Architecture of IA-32

Privilege Levels

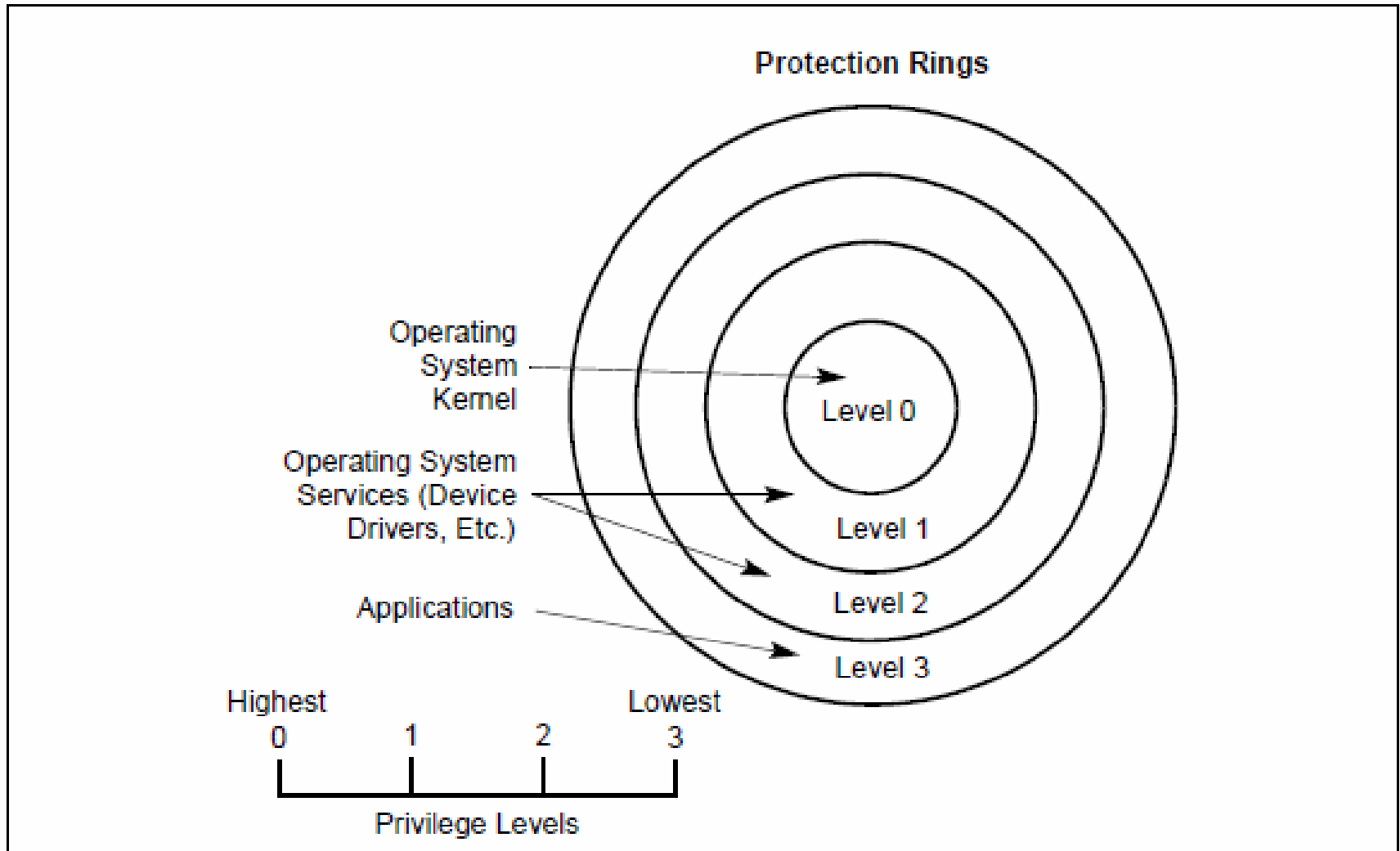


Figure 6-3. Protection Rings

Instruction Set Architecture of IA-32

Task

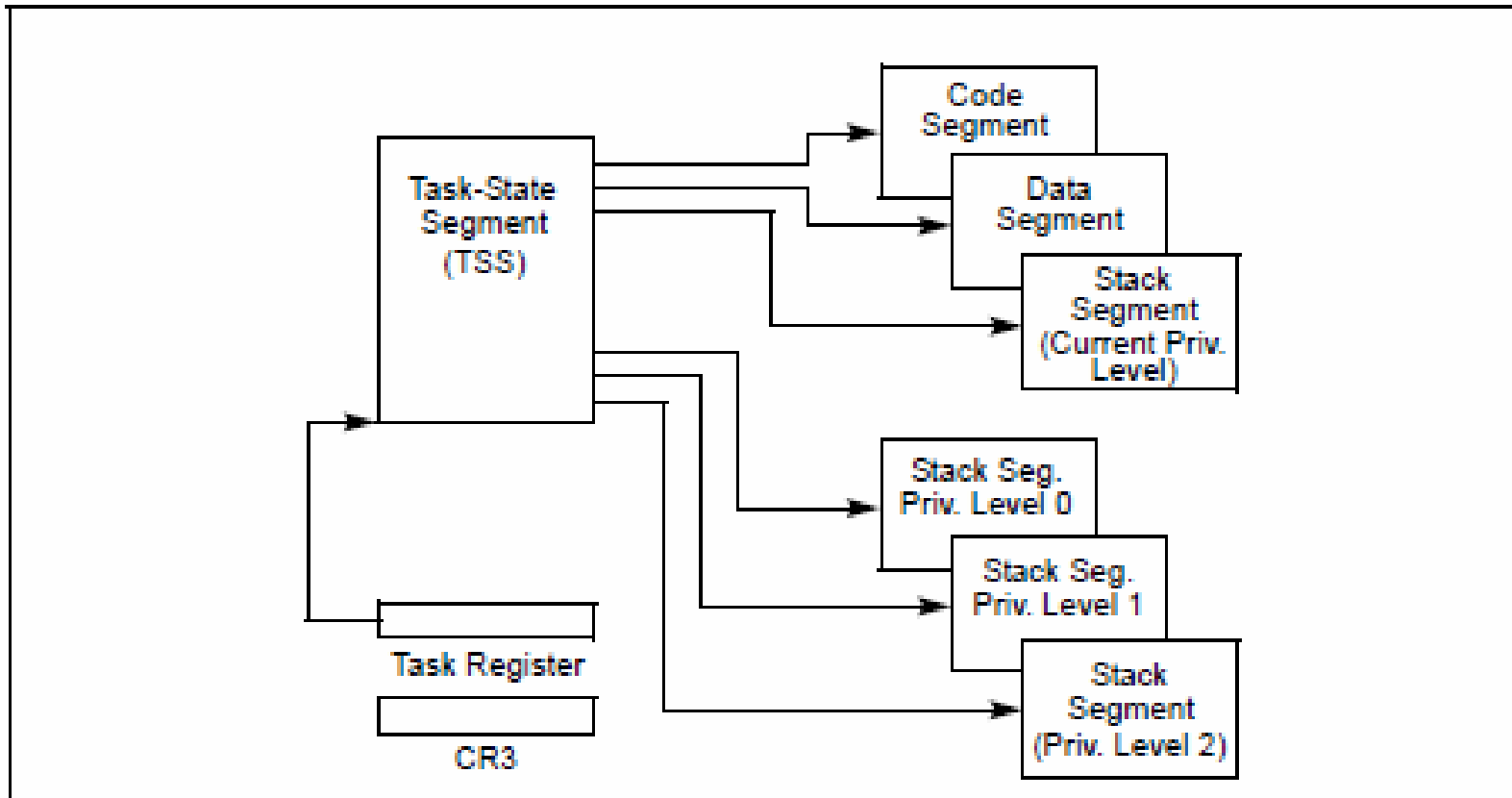


Figure 7-1. Structure of a Task

ISA of IA-32

Task- State Segment

31	15	0	
I/O Map Base Address		Reserved	T 100
Reserved		LDT Segment Selector	96
Reserved		GS	92
Reserved		FS	88
Reserved		DS	84
Reserved		SS	80
Reserved		CS	76
Reserved		ES	72
		EDI	68
		ESI	64
		EBP	60
		ESP	56
		EBX	52
		EDX	48
		ECX	44
		EAX	40
		EFLAGS	36
		EIP	32
		CR3 (PDBR)	28
Reserved		SS2	24
		ESP2	20
Reserved		SS1	16
		ESP1	12
Reserved		SS0	8
		ESP0	4
Reserved		Previous Task Link	0


 Reserved bits. Set to 0.

Figure 7-2. 32-Bit Task-State Segment (TSS)

ISA of IA-32

System-Level Registers and Data Structures devoted to Task Management

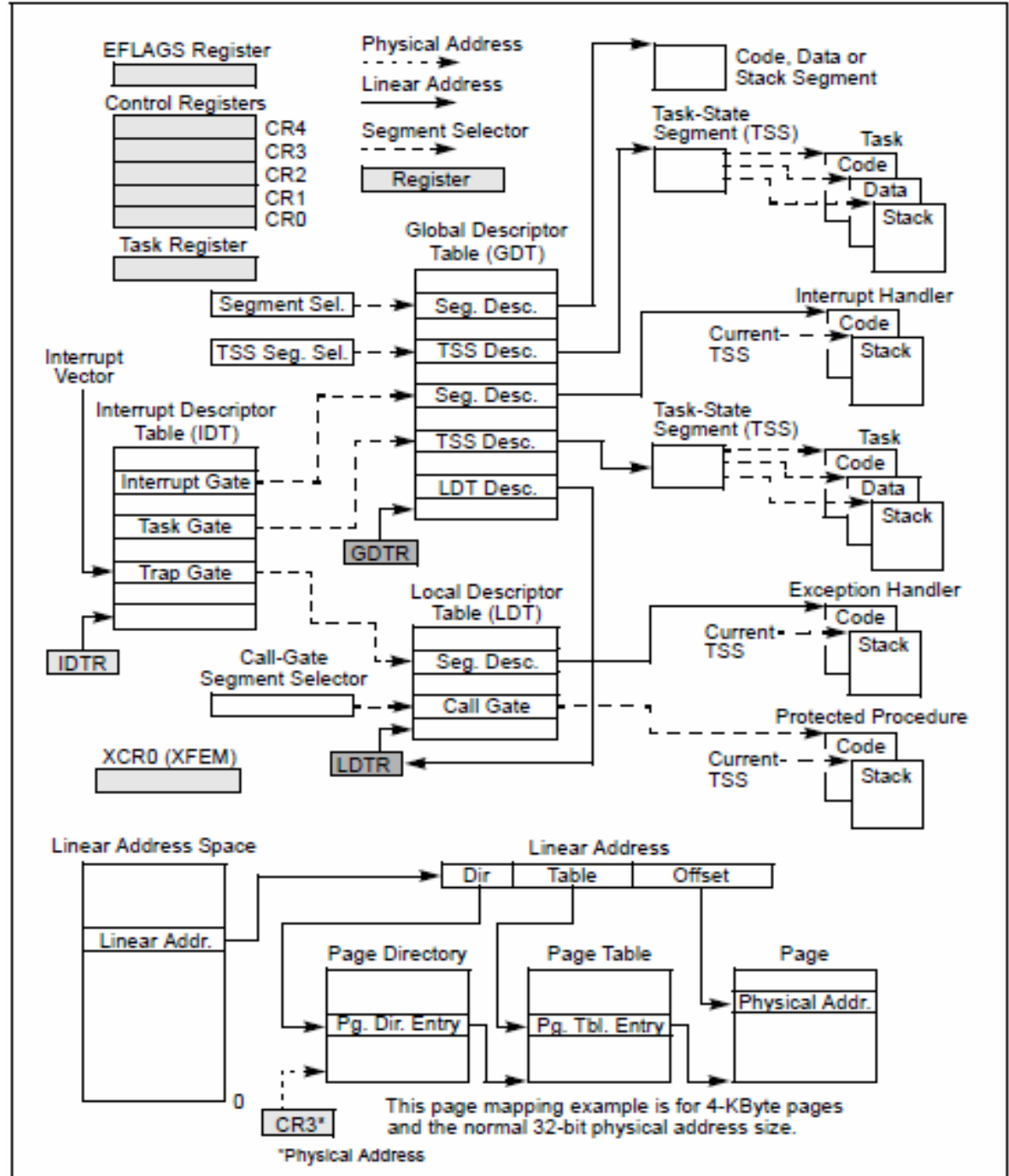


Figure 2-1. IA-32 System-Level Registers and Data Structures

ISA of IA-32

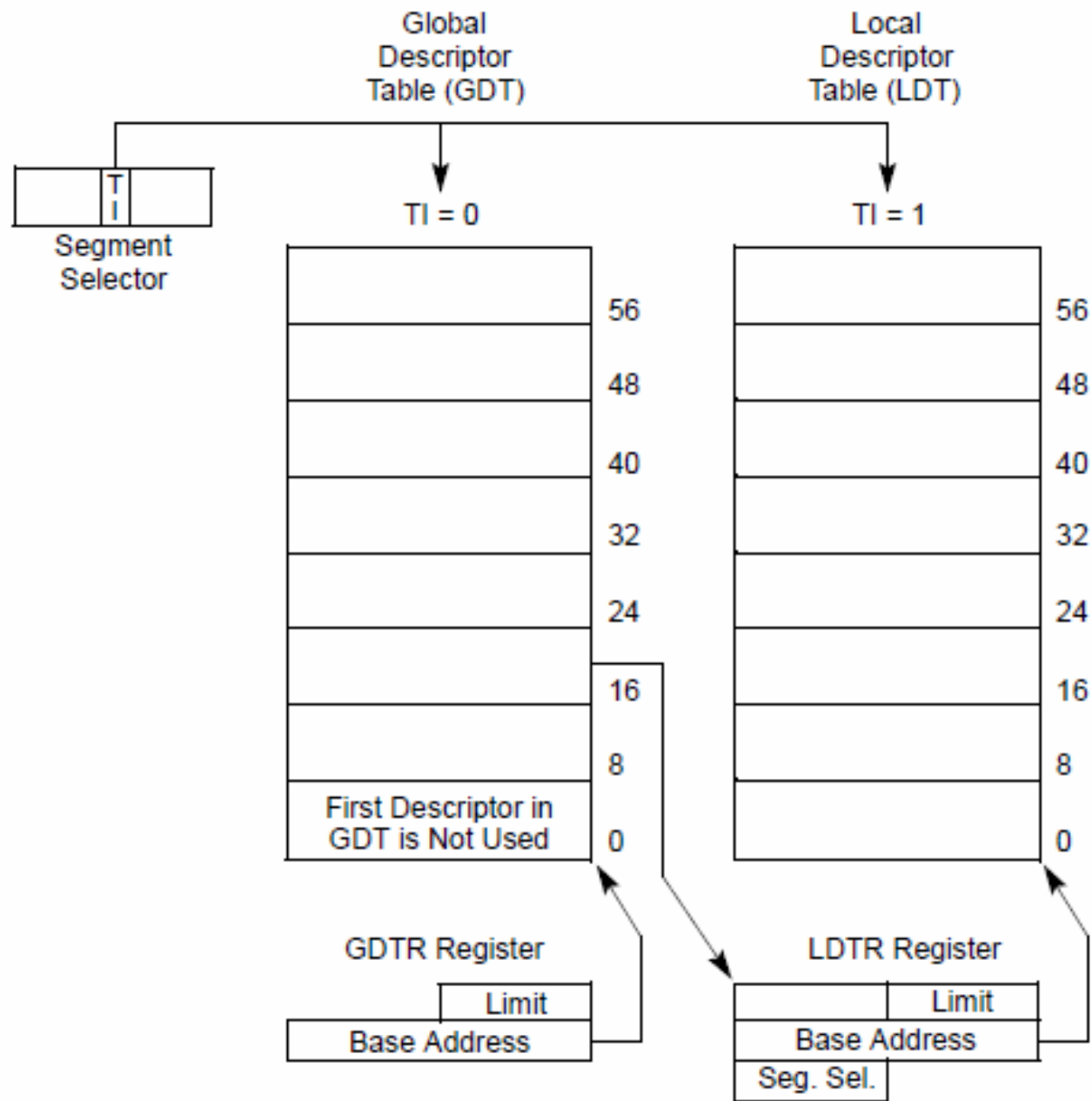


Figure 3-10. Global and Local Descriptor Tables

ISA – Segmentazione e Paginazione in IA-32

