START

C, A ← 0
M ← Multiplicand
Q ← Multiplier
Count ← $n$

$Q_0 = 1?$

No    Yes

C, A ← A + M

Shift C, A, Q
Count ← Count − 1

Count = 0?

No    Yes

END    Product in A, Q

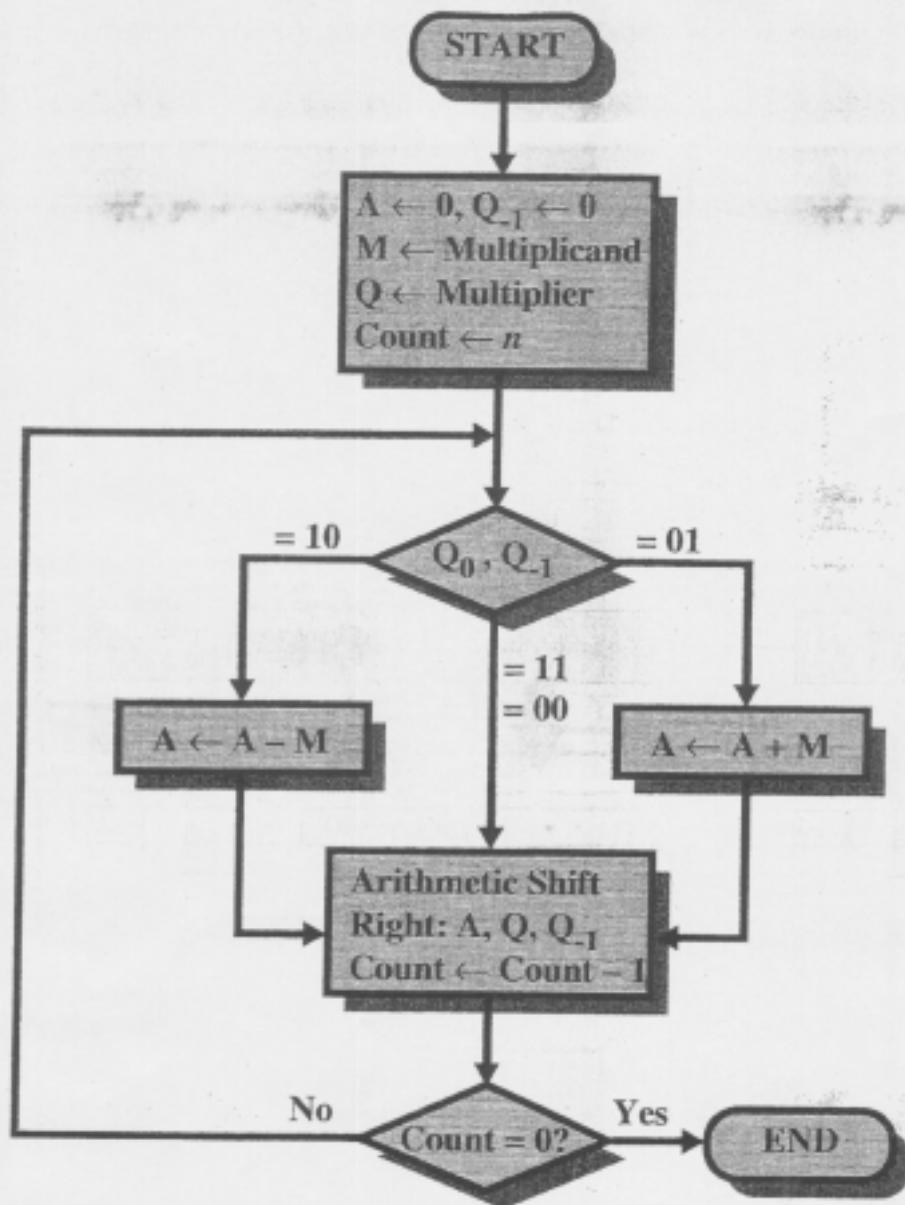**Figure 8.9**   Flowchart for Unsigned Binary Multiplication.

Multiplicand

$M_{n-1}$ · · · $M_0$

n-Bit Adder ← Add ← Shift and Add Control Logic

Shift Right

C → $A_{n-1}$ · · · $A_0$ → $Q_{n-1}$ · · · $Q_0$

Multiplier
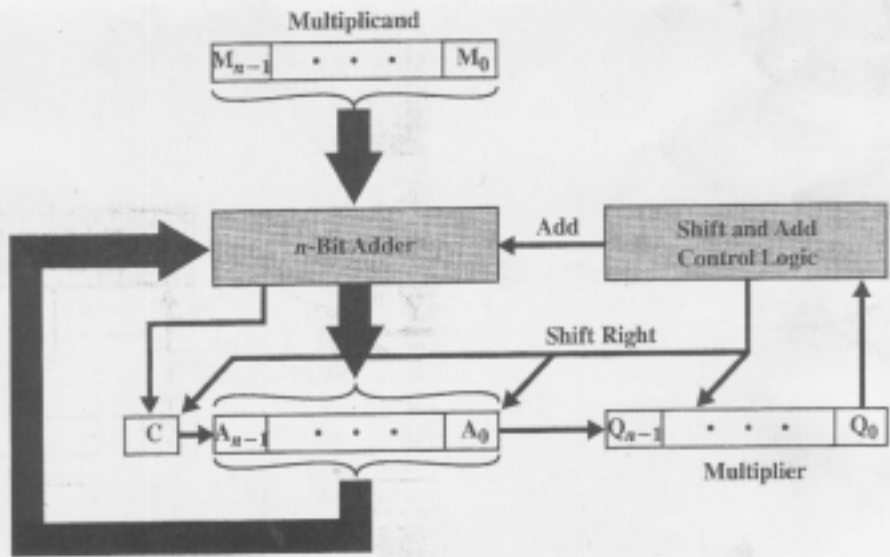
(a) Block Diagram

| C | A | Q | M | | |
|---|------|------|------|-----------|--------|
| 0 | 0000 | 1101 | 1011 | Initial Values | |
| 0 | 1011 | 1101 | 1011 | Add | First |
| 0 | 0101 | 1110 | 1011 | Shift | Cycle |
| 0 | 0010 | 1111 | 1011 | Shift | Second Cycle |
| 0 | 1101 | 1111 | 1011 | Add | Third |
| 0 | 0110 | 1111 | 1011 | Shift | Cycle |
| 1 | 0001 | 1111 | 1011 | Add | Fourth |
| 0 | 1000 | 1111 | 1011 | Shift | Cycle |

(b) Example from Figure 8.7 (product in A, Q)

**Figure 8.8** Hardware Implementation of Unsigned Binary Multiplication.

```
                        ┌──────────┐
                        │  START   │
                        └────┬─────┘
                             │
                             ▼
                  ┌────────────────────────┐
                  │ A ← 0, Q₋₁ ← 0          │
                  │ M ← Multiplicand        │
                  │ Q ← Multiplier          │
                  │ Count ← n               │
                  └──────────┬──────────────┘
                             │
     ┌───────────────────────┼───────────────────────┐
     │                       ▼                        │
     │        = 10      ╱ Q₀ , Q₋₁ ╲     = 01          │
     │       ┌──────────◄           ►──────────┐       │
     │       │          ╲           ╱          │       │
     │       │               = 11              │       │
     │       │               = 00              │       │
     │       ▼                  │              ▼       │
     │ ┌─────────────┐          │       ┌─────────────┐│
     │ │  A ← A − M  │          │       │  A ← A + M  ││
     │ └──────┬──────┘          │       └──────┬──────┘│
     │        │                 ▼              │       │
     │        │   ┌──────────────────────────┐ │       │
     │        └──►│ Arithmetic Shift          │◄┘       │
     │            │ Right: A, Q, Q₋₁          │         │
     │            │ Count ← Count − 1         │         │
     │            └────────────┬─────────────┘         │
     │                         │                       │
     │     No                  ▼           Yes         │
     └──────────────◄ Count = 0? ►──────────► END
```

**Figure 8.12**  Booth's Algorithm for Twos Complement
Multiplication.

| A | Q | $Q_{-1}$ | M | | |
|------|------|------|------|------|------|
| 0000 | 0011 | 0 | 0111 | Initial Values | |
| 1001 | 0011 | 0 | 0111 | A ← A − M | First |
| 1100 | 1001 | 1 | 0111 | Shift | Cycle |
| 1110 | 0100 | 1 | 0111 | Shift | Second Cycle |
| 0101 | 0100 | 1 | 0111 | A ← A + M | Third |
| 0010 | 1010 | 0 | 0111 | Shift | Cycle |
| 0001 | 0101 | 0 | 0111 | Shift | Fourth Cycle |

**Figure 8.13** Example of Booth's Algorithm.